SonicBOOM Current and Future

ADEPT EoP Party

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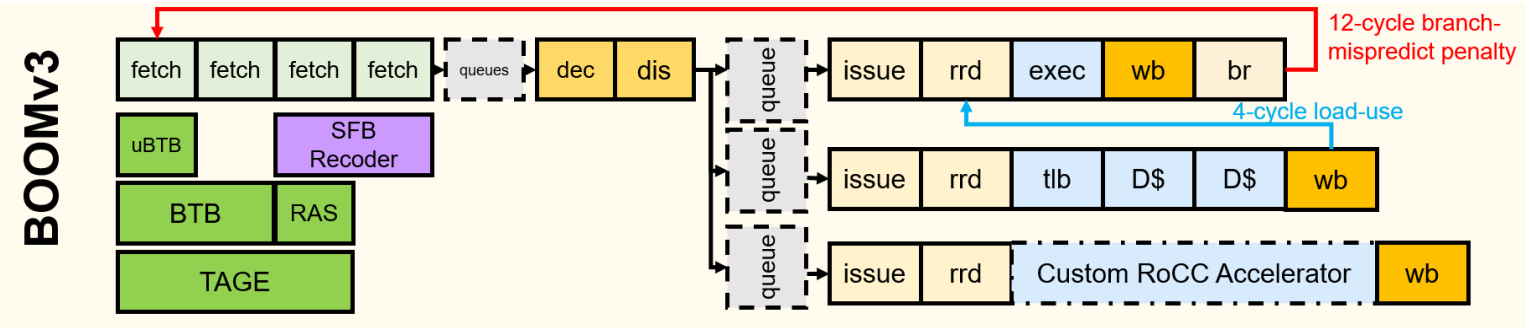
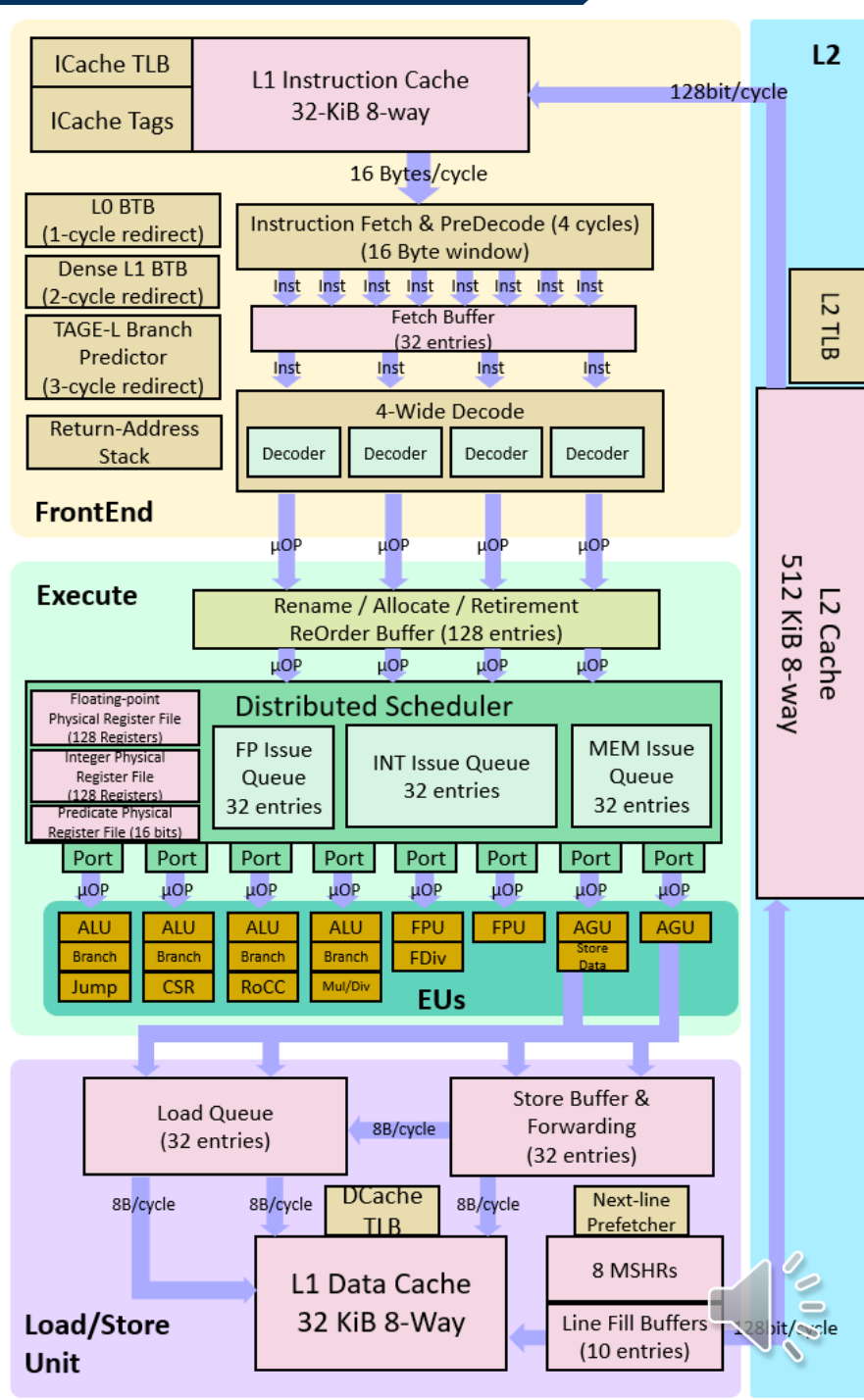
Berkeley Architecture Research

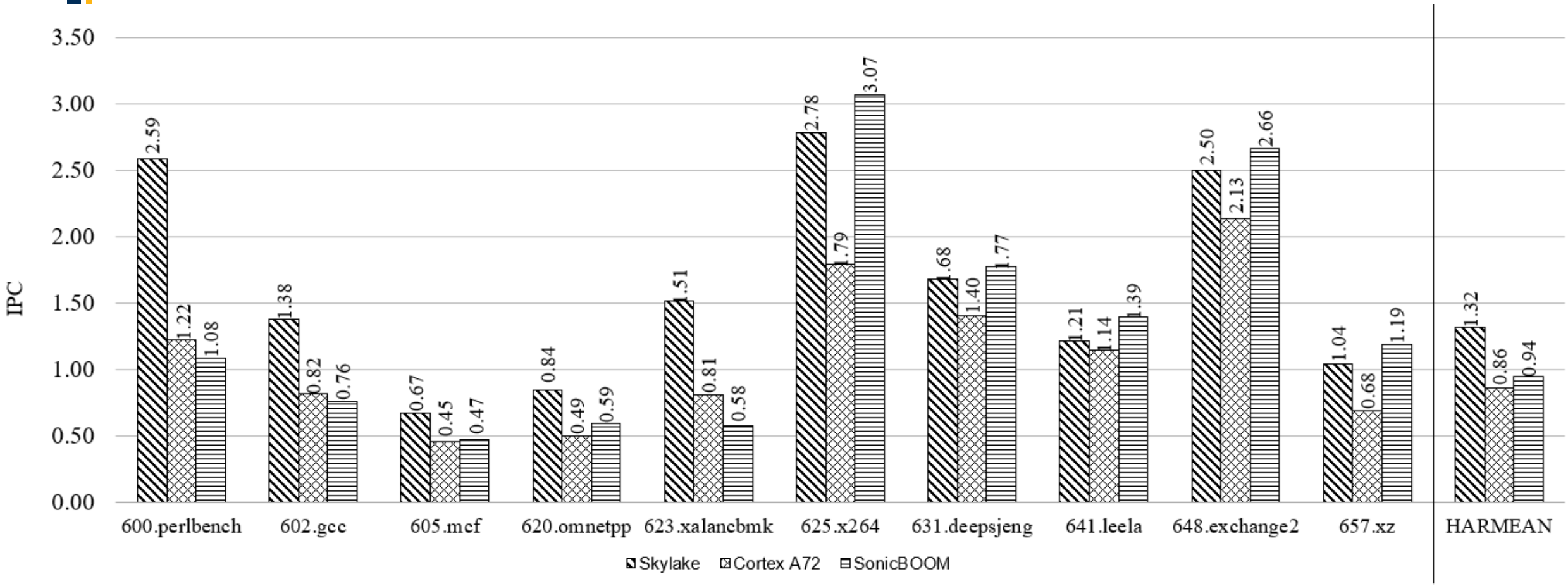
A High-performance OOO Core

- Comparable in features/performance to commercial cores
- **Advanced frontend**: TAGE-based branch predictor
- **Scalable backend**: banked execution clusters + extensible w. custom functional units
- **Wide load/store:** multi-issue non-blocking OOO load-store unit





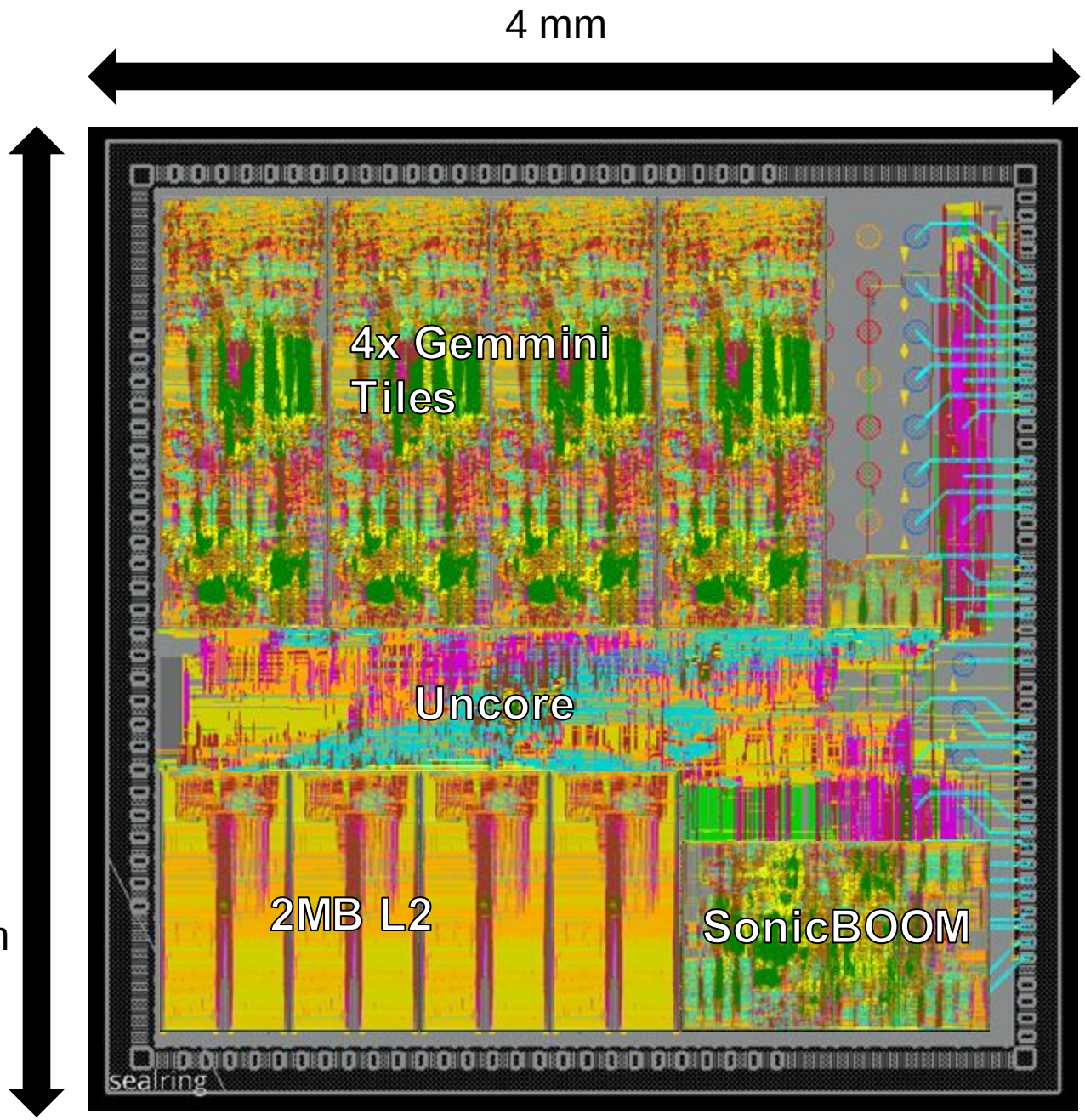
SPEC17 results



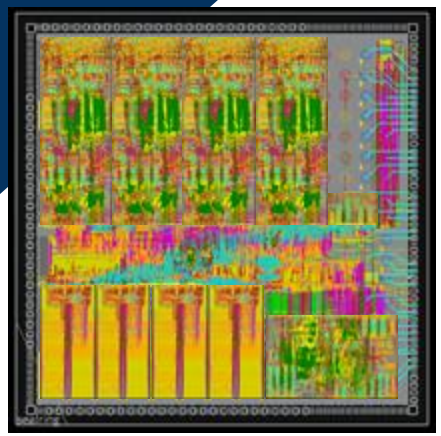
ARGO:

Architecture for **R**eal-time ML with **G**emminis and a **O**ut-of-order core

- Test chip with features for Real Time Machine Learning
- 16 mm^2 in GF 12nm
- Multi-core systolic arrays with training and inference support
- 9-wide out-of-order RISC-V core
- Built on Chipyard/HAMMER for agile, rapid design



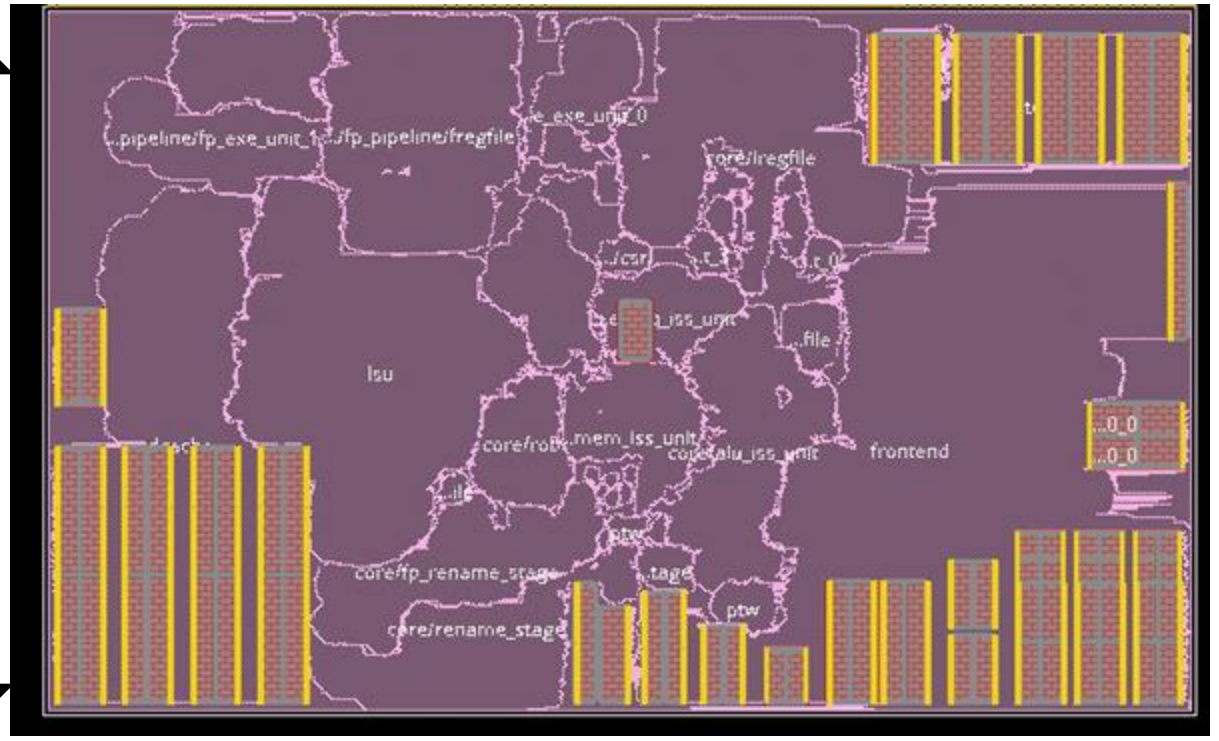
Taped-out in ARGO chip



- 9-wide OOO tapeout
- 1 mm^2 on GF12nm
- 1.2 GHz at 0.72V SS
- Critical paths through DCache/ICache

1.3 mm

0.8 mm



SonicBOOM Tile

TAGE	5x INT ALUs	Dual-issue LSU
32KB L1I$	2x FP64 MACs	272-entry PRF
32KB L1D$		

Testimonials

"Open-Source Cores [BOOM] **Quite Capable** … Open source implies low cost… not necessarily low performance" – *DAC58 OpenSoC Tutorial*

"**State-of-the-Art** – BOOMv3.
Arguably the **most advanced open-source RISC-V CPU**" – *DAC58 OpenSoC Tutorial*

"BOOM achieves the highest ASIC processing performance [of selected open-source RISC-V cores]... **best-in-class** for ASIC performance" – *Dorflinger, et al., A Comparative Survey of Open-Source Application-Class RISC-V Processor Implementations.*

"If you want to see **what non-trivial branch prediction, cache management, instruction decoding and scheduling, and out-of-order execution** look like under the hood, it's all there for you." – *The Register*

"**Extremely valuable asset** during quarantine" – */u/hdante*

Academic Impact

- **Chris's Thesis**: 40 citations
- **SonicBOOM**, *CARRV '20*: 24 citations
- **Mitigating Spectre on BOOM**, *CARRV '19*: 12 citations
  - Used in CS152 class lab – implement+execute Spectre in ~2 weeks
- University of Cambridge Computer Architecture course readings:

Lecture 5 and 6 - Superscalar processors

The Alpha and MIPS processors below are older, but have influenced modern designs. The papers are also full of interesting information and are written in a way that makes them quite accessible.

R. E. Kessler, "The Alpha 21264 microprocessor", IEEE Micro, 19(2), Mar/Apr 1999. (article)

K. C. Yeager, "The MIPS R10000 Superscalar Microprocessor", IEEE Micro, 16(2), Apr 1996. (article)

J. Zhao, B. Korpan, A. Gonzalez, K. Asanovic, "SonicBoom: The 3rd generation Berkely Out-of-Order Machine", (article) (further technical documentation)

BOOM Future in SLICE

- Can't "move fast and break things" any more ...
  users expect SPEC17 to work
- Diminishing ROI on microarchitecture work ...
  no low-hanging fruit remaining

But...

- Still some features hanging in the development pipe
- Considering integration of future features
- Continue to use as a high-performance baseline core