Verification

developed during

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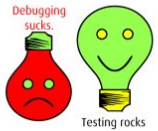
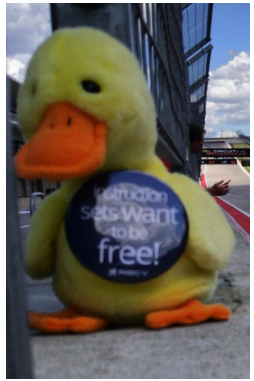


Improving Chisel Testing

*improve test economy with the **Chisel stimulus package***

CHISEL
COALIATION *for*
STANDARDIZED TESTING



- **chiseltest** library started by Richard Lin in 2018
- write simulator independent test benches in Scala
- safe multi-threading for decoupled test components

Andrew Dobis, Tjark Petersen, Hans Jakob Damsgaard, Kasper Juul Hesse Rasmussen, Enrico Tolotto, Simon Thye Andersen, **Richard Lin**, and Martin Schoeberl.
"Chiselverify: An open-source hardware verification library for chisel and scala."
In *2021 IEEE Nordic Circuits and Systems Conference (NorCAS)*

Open-Source Formal Verification for Chisel

Kevin Laeufer, Jonathan Bachrach and Koushik Sen
Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, USA
Email: {laeufer, jrb, ksen}@eecs.berkeley.edu

Workshop on Open-Source EDA Technology (WOSET) **2021**.

- formal property checks using only open-source tools
- part of **chiseltest** in the upcoming Chisel 3.5 release

Simulator Independent Coverage for RTL Hardware Languages

Kevin Laeufer, Vighnesh Iyer, David Biancolin, Jonathan Bachrach, Borivoje Nikolic and Koushik Sen
EECS Department
University of California, Berkeley, USA
{laeufer,vighnesh.iyer,biancolin,jrb,bora,ksen}@eecs.berkeley.edu

Currently under submission.

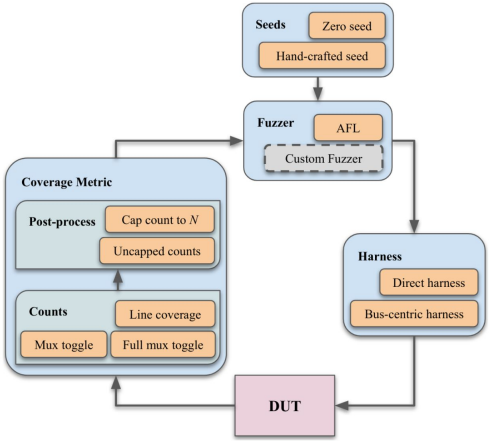
- native line, toggle, fsm coverage for Chisel circuits
- works on Verilator, treadle, FireSim, ESSENT and more
- merge coverage across simulators
- fuzzing

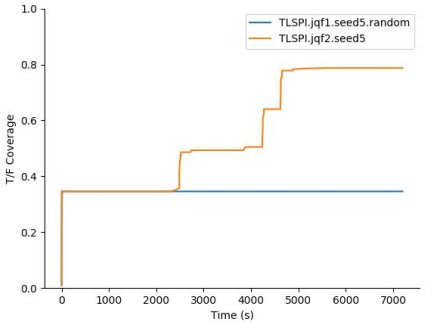
Hardware Fuzzing

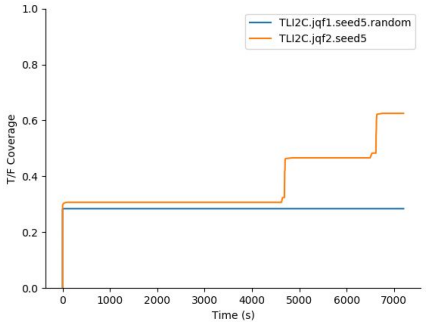
Laeufer, Kevin, Jack Koenig, Donggyu Kim, Jonathan Bachrach, and Koushik Sen.
"RFUZZ: Coverage-directed fuzz testing of RTL on FPGAs."
In *2018 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*.

- many follow up works from other groups

Brandon Fajardo, **Kevin Laeufer,** Jonathan Bachrach, and Koushik Sen.
"RTLFUZZLAB: Building A Modular Open-Source Hardware Fuzzing Framework."
Workshop on Open-Source EDA Technology (WOSET) 2021.





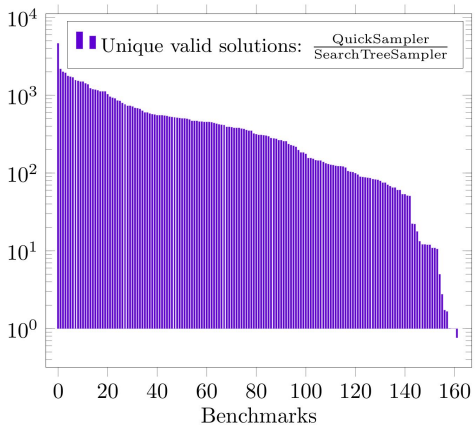


Quicksampler

Rafael Dutra, Kevin Laeufer, Jonathan Bachrach, and Koushik Sen. "Efficient sampling of SAT solutions for testing." In *2018 IEEE/ACM 40th International Conference on Software Engineering (ICSE)*, 2018.

+ 2 followup papers extending technique to SMT and weighted SMT

- used by Stanford in the **fault** verification library
- also implemented by us as part of our **verif** Chisel verification framework

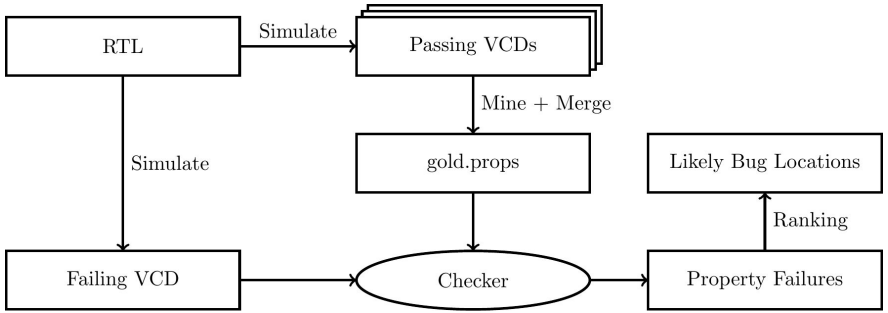


10^2 to 10^5 times faster than previous techniques

Specification Mining

Vighnesh Iyer, Donggyu Kim, Borivoje Nikolic, and Sanjit Seshia. "RTL Bug Localization Through LTL Specification Mining."
In *2019 ACM-IEEE International Conference on Formal Methods and Models for System Design (MEMOCODE)*.

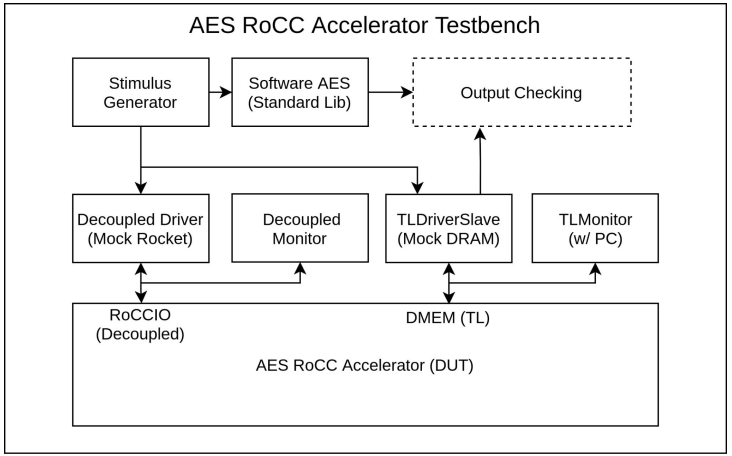
- Can we localize RTL bugs by mining specifications on passing tests?
- Demonstrated bug localization on riscv-mini

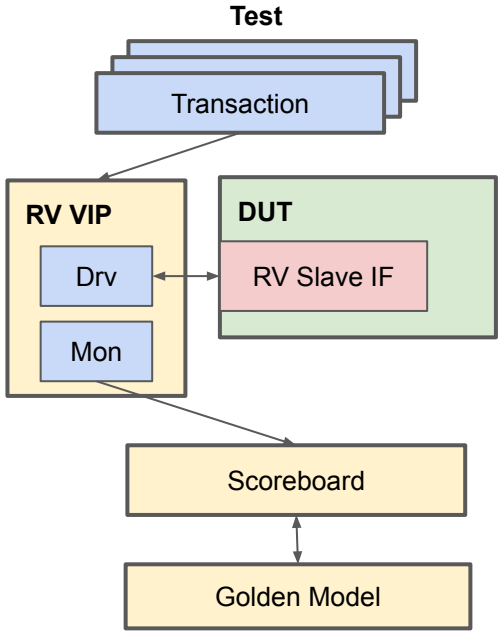


Dynamic Verification Library for Chisel

Anson Tsai. "Technical Report: Dynamic Verification Library for Chisel."

- Development of transaction-level TileLink VIPs using chiseltest
- Full UVM-like testbench environment in Scala
- Specification language over concrete traces
- Dynamic verification setups of RoCC accelerators and L2 cache

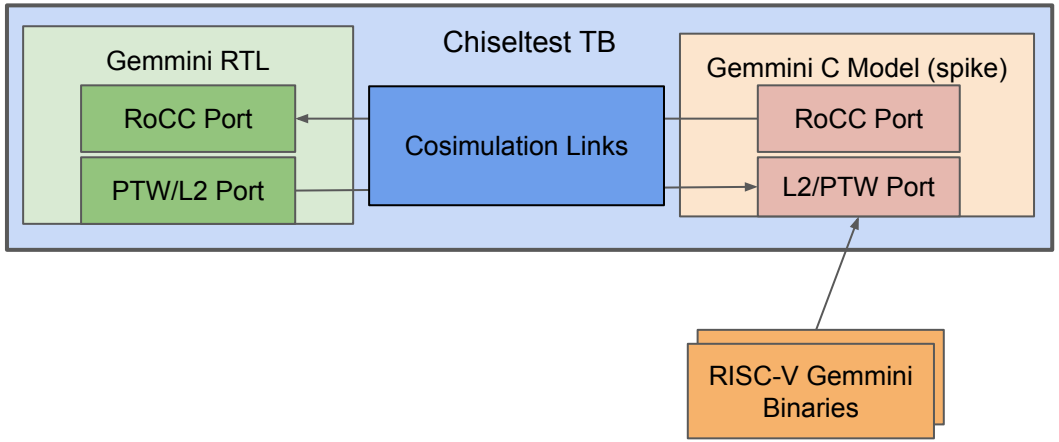




CoSimulation Framework for Chisel

Ryan Lund. "Technical Report: Design and Application of a Co-Simulation Framework for Chisel."

- Cosimulation framework using chiseltest for RTL and spike as RISC-V ISA model
- Proof of concept with Gemmini RoCC accelerator
- Up to 10x simulation runtime speedup



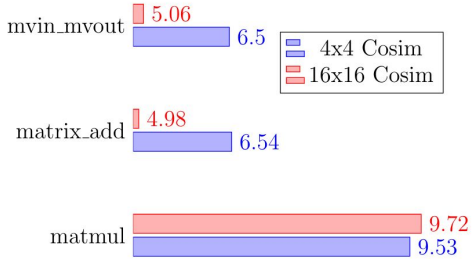


Figure 12: Avg. test speedup relative to full-SoC simulation.