Verification

developed during

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Improving Chisel Testing

improve test economy with the Chisel stimulus package

- **chiseltest** library started by Richard Lin in 2018
- write simulator independent test benches in Scala
- safe multi-threading for decoupled test components

Andrew Dobis, Tjark Petersen, Hans Jakob Damsgaard, Kasper Juul Hesse Rasmussen, Enrico Tolotto, Simon Thye Andersen, **Richard Lin**, and Martin Schoeberl.

"Chiselverify: An open-source hardware verification library for chisel and scala."

In *2021 IEEE Nordic Circuits and Systems Conference (NorCAS)*
Open-Source Formal Verification for Chisel

Kevin Laeufer, Jonathan Bachrach and Koushik Sen
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Workshop on Open-Source EDA Technology (WOSET) 2021.

- formal property checks using only open-source tools
- part of chiselttest in the upcoming Chisel 3.5 release
Simulator Independent Coverage for RTL Hardware Languages

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Currently under submission.

- native line, toggle, fsm coverage for Chisel circuits
- works on Verilator, treadle, FireSim, ESSENT and more
- merge coverage across simulators
- fuzzing
Hardware Fuzzing


- many follow up works from other groups

Quicksampler


+ 2 followup papers extending technique to SMT and weighted SMT

- used by Stanford in the fault verification library
- also implemented by us as part of our verif Chisel verification framework

10^2 to 10^5 times faster than previous techniques
Can we localize RTL bugs by mining specifications on passing tests?

Demonstrated bug localization on riscv-mini
Dynamic Verification Library for Chisel


- Development of transaction-level TileLink VIPs using chiselttest
- Full UVM-like testbench environment in Scala
- Specification language over concrete traces
- Dynamic verification setups of RoCC accelerators and L2 cache
CoSimulation Framework for Chisel


- Cosimulation framework using chiseltest for RTL and spike as RISC-V ISA model
- Proof of concept with Gemmini RoCC accelerator
- Up to 10x simulation runtime speedup