BEAGLE

Berkeley SoC Components in Intel 22FFL

ADEPT End of Project 12/9/2021

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A Perfect Storm...

Adapted from Krste’s “Semiconductor Industry Perfect Storm” Slide
A Perfect Storm…

“Cold Air”
Older graduate students and prior BOOM developers who have intimate tapeout knowledge are leaving.
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“Hot Air”
New graduate students incoming!
More components than ever to make interesting chips!

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BEAGLE = BOOM + EAGLE

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A BEAGLE is born

Goals

• Tapeout Intel 22FFL
• Second BOOM chip
  • Updated BOOMv2.2 core
  • Done with a completely new team
    • Jerry Z., Ben K., and more
• Create first multi-core heterogeneous system with Chipyard-like ecosystem
  • BOOM + Rocket
  • Gemmini + Hwacha
  • L2 + Serial Links + IOs
• Two compute domains and uncore
  • Each with separate asynchronous clock/power domains
General Application Domain

- Updated BOOMv2.2 - RVC, RoCC accel. support, Non-speculative mode
- Hwacha Vector Accelerator
Machine Learning Domain

- Rocket In-Order Core
- Gemmini DNN Accelerator
Uncore Domain

- Shared 1MB L2
- Configurable clock div./muxes

- GPIO, UART, SPI, I2C, JTAG
- Low-speed SerDes
GDS Photo

4mm x 4mm

~2.5mm
Test/Board Setup
# Runs Linux + More!

<table>
<thead>
<tr>
<th>Core Type</th>
<th>CoreMark</th>
<th>CoreMark/MHz</th>
<th>Dhrystone/S</th>
<th>DMIPS/MHz</th>
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<tbody>
<tr>
<td>Rocket</td>
<td>1185</td>
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<td>1883.54</td>
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<td>BOOM</td>
<td>Non-Speculative</td>
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<td>Full/Normal</td>
<td>395.79</td>
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Takeaways

• Published at ESSCIRC 2021:
  • A 16mm² 106.1 GOPS/W Heterogeneous RISC-V Multi-Core Multi-Accelerator SoC in Low-Power 22nm FinFET

• Developed in parallel with 1st Chipyard framework
  • 2nd BOOM tapeout – with new BOOM and new people!
  • Added Hwacha, Gemmini, and open-source L2!
  • Demonstrates booting real workloads!

• Giving back to future chips
  • Added a bringup flow to Chipyard
  • Added a lot of test-chip test features into Chipyard
  • Added an FPGA prototyping flow
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